COMPLETE LISTING OF CLAIMS IN THE CASE

Please amend Claims 1, 4, 7, and10 as follows:

1. (Currently Amended) A semiconductor device having a N-gate/N-substrate capacitor for characterizing polysilicon gate depletion corresponding to the semiconductor device, comprising:

an N doped substrate;

a gate oxide layer disposed over the N doped substrate;;

a first isolation oxide and a second isolation oxide disposed over the N doped substrate, wherein the first isolation oxide and the second isolation oxide are separated by ~~and on opposing edges of~~ the gate oxide layer;

an N+ doped gate disposed over at least one portion of the first isolation oxide, the gate oxide, and the second isolation oxide.

2. (Original) The semiconductor device of Claim 1, wherein the gate is in a depletion mode simultaneously while the N doped substrate is in an accumulation mode.

3. (Original) The semiconductor device of Claim 1, wherein the polysilicon gate depletion of the semiconductor device corresponds to capacitor-voltage characteristics of the N-gate/N-substrate capacitor.

4. (Previously Presented) A semiconductor device having a P-gate/P-substrate capacitor for characterizing polysilicon gate depletion corresponding to the semiconductor device, comprising:

a P doped substrate;

a gate oxide layer disposed over the P doped substrate;

a first isolation oxide and a second isolation oxide disposed over the P doped substrate;

a P+ doped gate disposed over at least one portion of the first isolation oxide, the gate oxide, and the second isolation oxide.

5. (Original) The semiconductor device of Claim 4, wherein the gate is in a depletion mode simultaneously while the substrate is in an accumulation mode.

6. (Original) The semiconductor device of Claim 4, wherein the polysilicon gate depletion of the semiconductor device corresponds to capacitor-voltage characteristics of the P-gate/P-substrate capacitor.

7. (Previously Presented) A semiconductor capacitor structure, comprising:

an N doped substrate;

a gate oxide layer disposed over the substrate;

a first isolation oxide and a second isolation oxide disposed over the substrate;

an N+ doped gate disposed over the first isolation oxide, the gate oxide, and the second isolation oxide, wherein the semiconductor capacitor is used to characterize polysilicon gate depletion corresponding to a semiconductor fabrication process.

8. (Original) The semiconductor capacitor of Claim 7, wherein the gate is in a depletion mode while the substrate is an accumulation mode.

9. (Original) The semiconductor structure of Claim 7, wherein the polysilicon gate depletion corresponding to the semiconductor fabrication process is characterized by capacitor-voltage characteristics of the semiconductor capacitor.

10. (Previously Presented) A semiconductor capacitor structure, comprising:

an P doped substrate;

a gate oxide layer disposed over the substrate;

a first isolation oxide and a second isolation oxide disposed over the substrate;

a P+ doped gate disposed over the first isolation oxide, the gate oxide, and the second isolation oxide, wherein the semiconductor capacitor structure is used to characterize polysilicon gate depletion corresponding to a semiconductor process.

11. (Original) The semiconductor device of Claim 10, wherein the gate is driven into depletion while the substrate is simultaneously driven into accumulation.

12. (Original) The semiconductor device of Claim 10, wherein capacitance-voltage measurements are taken to characterize the polysilicon gate depletion of the semiconductor device.

Claims 13-20 (canceled)